

Introduction

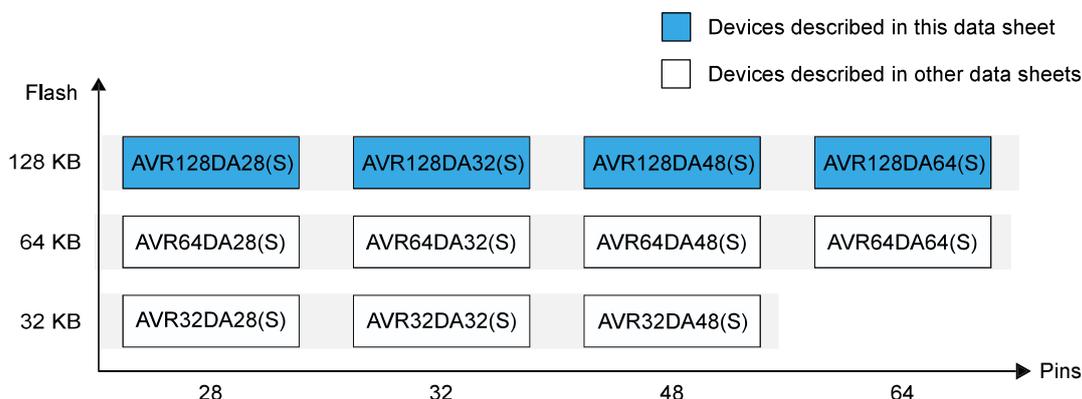
The AVR128DA28/32/48/64(S) microcontrollers of the AVR® DA family use the AVR CPU with hardware multiplier, running at up to 24 MHz, with 128 KB of Flash, 16 KB of SRAM, and 512B of EEPROM in 28-, 32-, 48- or 64-pin packages. The AVR® DA(S) family uses the latest technologies from Microchip Technology, with a flexible and low-power architecture including an Event System, intelligent analog features, advanced digital peripherals, and Peripheral Touch Controller (PTC).

AVR® DA(S) Family Overview

The figure below shows the AVR® DA(S) devices, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count, and therefore, the available features

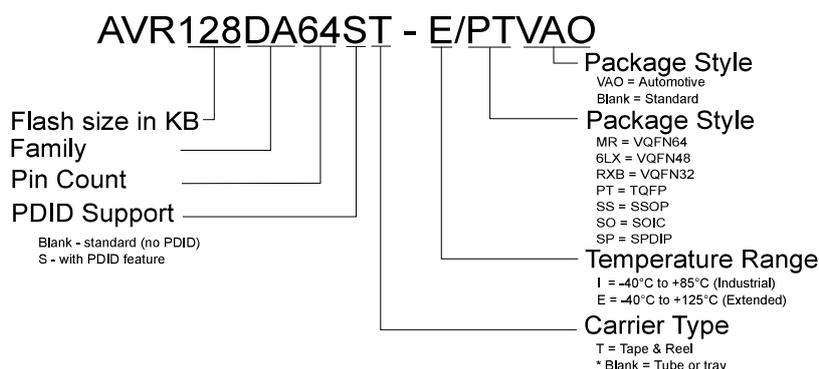
Figure 1. AVR® DA(S) Family Overview



Devices with different Flash memory sizes typically also have different SRAM.

The name of a device in the AVR® DA(S) family is decoded as follows:

Figure 2. AVR® DA(S) Device Designations



Memory Overview

The following table shows the memory overview of the entire family. Further documentation describes only the AVR128DA28/32/48/64(S) devices.

Table 1. Memory Overview

Devices	AVR32DA28(S) AVR32DA32(S) AVR32DA48(S)	AVR64DA28(S) AVR64DA32(S) AVR64DA48(S) AVR64DA64(S)	AVR128DA28(S) AVR128DA32(S) AVR128DA48(S) AVR128DA64(S)
Flash Memory	32 KB	64 KB	128 KB
SRAM	4 KB	8 KB	16 KB
EEPROM	512B	512B	512B
User Row	32B	32B	32B

Peripheral Overview

The following table shows the peripheral overview of the entire AVR® DA(S) family. Further documentation describes only the AVR128DA28/32/48/64(S) devices.

Table 2. Peripheral Overview

Feature	AVR128DA28(S) AVR64DA28(S) AVR32DA28(S)	AVR128DA32(S) AVR64DA32(S) AVR32DA32(S)	AVR128DA48(S) AVR64DA48(S) AVR32DA48(S)	AVR128DA64(S) AVR64DA64(S)
Pins	28	32	48	64
Max. Frequency (MHz)	24	24	24	24
16-bit Timer/Counter type A (TCA)	1	1	2	2
16-bit Timer/Counter type B (TCB)	3	3	4	5
12-bit Timer/Counter type D (TCD)	1	1	1	1
Real-Time Counter (RTC)	1	1	1	1
USART	3	3	5	6
SPI	2	2	2	2
TWI/I ² C	1 ⁽¹⁾	2 ⁽¹⁾	2 ⁽¹⁾	2 ⁽¹⁾
12-bit Differential ADC (channels)	1 (10)	1 (14)	1 (18)	1 (22)
10-bit DA(S)C (outputs)	1(1)	1(1)	1(1)	1(1)
Analogue Comparator (AC)	3	3	3	3
Zero-Cross Detectors (ZCD)	1	1	2	3

.....continued				
Feature	AVR128DA28(S) AVR64DA28(S) AVR32DA28(S)	AVR128DA32(S) AVR64DA32(S) AVR32DA32(S)	AVR128DA48(S) AVR64DA48(S) AVR32DA48(S)	AVR128DA64(S) AVR64DA64(S)
Pins	28	32	48	64
Peripheral Touch Controller (PTC) (self-cap/ mutual cap channels)	1 (18/81)	1 (22/121)	1 (32/256)	1 (46/529)
Configurable Custom Logic (CCL)	1(4)	1(4)	1(6)	1(6)
Watchdog Timer (WDT)	1	1	1	1
Event System channels	8	8	10	10
General Purpose I/O ⁽²⁾	23 ⁽²⁾	27 ⁽²⁾	41 ⁽²⁾	55 ⁽²⁾
PORT	PA[7:0], PC[3:0], PD[7:0], PF[6,1,0]	PA[7:0], PC[3:0], PD[7:0], PF[6:0]	PA[7:0], PB[5:0], PC[7:0], PD[7:0], PE[3:0], PF[6:0]	PA[7:0], PB[7:0], PC[7:0], PD[7:0], PE[7:0], PF[6:0], PG[7:0]
External Interrupts	23	27	41	55
CRCSCAN	1	1	1	1
Unified Program and Debug Interface (UPDI)	1	1	1	1

Notes:

1. The TWI/I²C can operate simultaneously as host and client on different pins.
2. PF6/ $\overline{\text{RESET}}$ pin is input-only.

Security Concept

The AVR® DAS devices from the AVR® DA(S) family are general purpose microcontrollers that offer fundamental security features to implement secure firmware upgrades and authenticate the application firmware. When using the security features correctly, they protect against remote attacks and some PCB-level attacks where the application code is modified to change the product functionality.

The cornerstone of the security features is the *Program and Debug Interface Disable (PDID)*, a mechanism preventing access to the device's reprogrammable Flash memory over the Unified Program and Debug Interface (UPDI). After activating the PDID as described in the section *Memories*, the UPDI is prevented from making any changes to the device. The UPDI can still read out the device information and CRC status.

The only way to program the device after activating the PDID is by using software stored in the Boot Code section of the Flash to update the Application Code section software. This application-specific software must be able to receive new data and program the Application Code section. It is impossible to alter the code stored in the Boot Code section using this mechanism, as it is only accessible through the UPDI.

In addition, there is a separate storage space accessible only by code in the Boot Code section, which can hold any data intended to be accessible only from the Boot Code section. One example of this is a cryptographic key used to validate data sent to a bootloader to update the application software on the device.

This creates a two-layer security: The device is prevented from being erased or reprogrammed over the UPDI, and the code in the Boot Code section is protected. Secondly, the code in the Boot Code section can use a cryptographic key (that is only accessible by code in this section of Flash) to verify that any new application code that is received for the device software update is authentic.

Using the *Program and Debug Interface Disable (PDID)* in software requires cryptographic competencies to ensure conformity to cyber-security standards such as ISO/SAE DIS 21434.

Features

- AVR® CPU
 - Running at up to 24 MHz
 - Single-cycle I/O access
 - Two-level interrupt controller
 - Two-cycle hardware multiplier
 - Program and Debug Interface Disable (PDID) ⁽¹⁾
 - Supply voltage range: 1.8V to 5.5V
- Memories
 - 128 KB In-System self-programmable Flash memory
 - 512B EEPROM
 - 16 KB SRAM
 - 32B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
 - Write/erase endurance
 - Flash 1,000 cycles
 - EEPROM 100,000 cycles
 - Data retention: 40 years at 55°C
- System
 - Power-on Reset (POR) circuit
 - Brown-out Detector (BOD)
 - Clock options
 - High-Precision internal high-frequency Oscillator with selectable frequency up to 24 MHz (OSCHF)
 - Auto-tuning for improved internal oscillator accuracy
 - Internal PLL up to 48 MHz for high-frequency operation of Timer/Counter type D (PLL)
 - 32.768 kHz Ultra-Low Power internal oscillator (OSC32K)
 - 32.768 kHz external crystal oscillator (XOSC32K)
 - External clock input
 - Single-pin Unified Program and Debug Interface (UPDI)
 - Three sleep modes
 - Idle with all peripherals running for immediate wake-up
 - Standby with a configurable operation of selected peripherals
 - Power-Down with full data retention
- Peripherals
 - Up to two 16-bit Timer/Counter type A (TCA) with a dedicated period register and three PWM channels
 - Up to five 16-bit Timer/Counter type B (TCB) with input capture and simple PWM functionality
 - One 12-bit Timer/Counter type D (TCD) optimized for power control
 - One 16-bit Real-Time Counter (RTC) running from an external crystal or internal oscillator
 - Up to six USART with fractional baud rate generator, auto-baud, and start-of-frame detection
 - Two host/client Serial Peripheral Interface (SPI)

- Up to two Two-Wire Interface (TWI) with dual address match
 - Independent host and client operation (Dual mode)
 - Philips I²C compatible
 - Standard mode (Sm, 100 kHz)
 - Fast mode (Fm, 400 kHz)
 - Fast mode plus (Fm+, 1 MHz) ⁽²⁾
- Event System for CPU independent and predictable inter-peripheral signaling
- Configurable Custom Logic (CCL) with up to six programmable Look-up Tables (LUT)
- One 12-bit differential 130 ksps Analog-to-Digital Converter (ADC)
- Three Analog Comparators (ACs) with window compare functions
- One 10-bit Digital-to-Analog Converter (DAC)
- Up to three Zero-Cross Detectors (ZCD)
- Multiple voltage references (VREF)
 - 1.024V
 - 2.048V
 - 2.500V
 - 4.096V
- Peripheral Touch Controller (PTC) with Driven Shield+ and Boost Mode technologies for capacitive touch buttons, sliders, wheels and 2D surface
 - Up to 46 self-capacitance and 529 mutual capacitance channels
- Automated Cyclic Redundancy Check (CRC) Flash memory scan
- Watchdog Timer (WDT) with Window mode, with a separate on-chip oscillator
- External interrupt on all general purpose pins
- I/O and Packages:
 - Up to 55 programmable I/O pins
 - 28-pin SPDIP, SSOP and SOIC
 - 32-pin VQFN 5x5 mm and TQFP 7x7 mm
 - 48-pin VQFN 6x6 mm and TQFP 7x7 mm
 - 64-pin VQFN 9x9 mm and TQFP 10x10 mm
- Temperature Ranges:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C

Notes:

1. The PDID feature is available only for AVR® DAS devices.
2. I²C Fm+ is only supported for V_{DD} above 2.7V.