PIC16F17114/15/24/25/44/45 Full-Featured 8/14/20-Pin Microcontrollers

PIC16F17114/15/24/25/44/45

Introduction

The PIC16F171 microcontroller family has a suite of analog peripherals that enables precision sensor applications. This product family is available from 8 to 44-pin packages in a memory range of 7 KB to 28 KB, with speeds up to 32 MHz. This product includes a low-noise Operational Amplifier (Op-Amp), a 12-bit differential Analog-to-Digital Converter with Computation (ADCC), two 8-bit Digital-to-Analog Converters (DAC), up to four 16-bit Pulse-Width Modulation (PWM) peripherals, and many more waveform control and communication peripherals. This small form factor, feature-rich device is well suited for low-cost, energy-efficient analog sensor applications with higher resolution requirements.

PIC16F171 Family Summary

Table 1. Devices Included in This Data Sheet

Device	Program Flash Memory (bytes)	Data Flash Memory (EEPROM) (bytes)	Data SRAM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins(1)/ Peripheral Pin Select	8-Bit Timers with HLT/ 16-Bit Timers(2)	16-Bit PWM/ CCP	12-Bit ADC Channels (External+/External-/Internal)	I2C/SPI	EUSART	NCO	CWG	CLC	FVR	CMP	8-bit DAC	Operational Amplifier	ZCD	SMBus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Windowed Watchdog Timer
PIC16F17114	7K	128	512	Y/Y	6/Y	2/2	2/2	5/5/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	6	Y
PIC16F17115	14K	128	1024	Y/Y	6/Y	2/2	2/2	5/5/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	6	Y
PIC16F17124	7K	128	512	Y/Y	12/Y	2/2	2/2	11/11/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	12	Y
PIC16F17125	14K	128	1024	Y/Y	12/Y	2/2	2/2	11/11/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	12	Y
PIC16F17144	7K	128	512	Y/Y	18/Y	2/2	2/2	17/17/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	18	Y
PIC16F17145	14K	128	1024	Y/Y	18/Y	2/2	2/2	17/17/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	18	Y

Table 2. Devices Not Included in This Data Sheet

Device	Program Flash Memory (bytes)	Data Flash Memory (EEPROM) (bytes)	Data SRAM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins[1]/ Peripheral Pin Select	8-Bit Timers with HLT/ 16-Bit Timers[2]	16-Bit PWM/ CCP	12-Bit ADC Channels (External+/External-/Internal)	I2C/SPI	EUSART	NCO	CWG	CLC	FVR	CMP	8-bit DAC	Operational Amplifier	ZCD	SMBus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Watchdog Timer
PIC16F17126	28K	256	2048	Y/Y	12/Y	2/2	2/2	11/11/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	12	Y
PIC16F17146	28K	256	2048	Y/Y	18/Y	2/2	2/2	17/17/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	18	Y
PIC16F17154	7K	128	512	Y/Y	25/Y	3/2	4/2	24/11/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	25	Y
PIC16F17155	14K	128	1024	Y/Y	25/Y	3/2	4/2	24/11/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	25	Y
PIC16F17156	28K	256	2048	Y/Y	25/Y	3/2	4/2	24/11/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	25	Y
PIC16F17174	7K	128	512	Y/Y	36/Y	3/2	4/2	35/16/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	25	Y
PIC16F17175	14K	128	1024	Y/Y	36/Y	3/2	4/2	35/16/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	25	Y
PIC16F17176	28K	256	2048	Y/Y	36/Y	3/2	4/2	35/16/7	2/2	2	1	1	4	2	2	2	1	1	Y	1	25	Y

Notes:

1. Total I/O count includes one input-only pin ($\overline{\text{MCLR}}$).
2. Timer0 can be configured as either an 8 or 16-bit timer.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction time
- 16-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power Brown-out Reset (LPBOR)
- Windowed Watchdog Timer (WWDT)

Memory

- Up to 28 KB of Program Flash Memory
- Up to 2 KB of Data SRAM Memory
- Up to 256 Bytes of Data EEPROM Memory
- Memory Access Partition (MAP) with Program Flash Memory Partitioned into:
  - Application block
  - Boot block
  - Storage Area Flash (SAF) block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:

  - Temperature Indicator calibration coefficients
  - Fixed Voltage Reference (FVR) measurement data
  - Microchip Unique Identifier (MUI)
- Device Characteristics Information (DCI) Stores:
  - Program/erase row sizes
  - Pin count details
- Direct, Indirect, and Relative Addressing Modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep:
  - Lowest power consumption
  - Reduce system electrical noise while performing ADC conversions
- Peripheral Module Disable (PMD): Selectively Minimize the Active Power Consumption of Unused Peripherals
- Low-Power Mode Features:
  - Sleep current:
    - < 900 nA typical @ 3V/25°C (WDT enabled)
    - < 600 nA typical @ 3V/25°C (WDT disabled)
  - Operating current:
    - 48 µA typical @ 32 kHz, 3V/25°C
    - < 1 mA typical @ 4 MHz, 5V/25°C

Digital Peripherals

- Two Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Up to Four Pulse-Width Modulators (PWM):
  - 16-bit resolution
  - Independent pulse outputs
  - External Reset Signal (ERS) inputs
- Four Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- One Complimentary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources

  - Programmable dead band
  - Fault-shutdown input
- One Configurable 8/16-Bit Timer (TMR0)
- Two 16-Bit Timers (TMR1/3) with Gate Control
- Up to Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- One Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input clock up to 64 MHz
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 32-bit CRC over any portion of Program Flash Memory
- Two Enhanced Universal Synchronous Asynchronous Receiver Transmitters (EUSART):
  - RS-232, RS-485, LIN compatible
  - Auto-wake-up on Start
- Two Host Synchronous Serial Ports (MSSP):
  - Serial Peripheral Interface (SPI) mode
    - Chip Select Synchronization
  - Inter-Integrated Circuit (I^2C) mode
    - 7/10-bit Addressing modes
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Device I/O Port Features:
  - Up to 35 I/O pins
  - One input-only pin
  - Individual I/O direction, open-drain, input threshold, slew rate, and weak pull-up control
  - Interrupt-on-Change (IOC) on up to 25 pins
  - One external interrupt pin

Analog Peripherals

- Differential Analog-to-Digital Converter with Computation (ADCC):
  - 12-bit resolution
  - Up to 35 external positive input channels
  - Up to 17 external negative input channels
  - Seven internal input channels
  - Internal ADC oscillator (ADCRC)
  - Operates in Sleep
  - Selectable Auto-Conversion Trigger (ACT) sources
- Two 8-Bit Digital-to-Analog Converters (DAC):
  - Output available on up to two I/O pins
  - Internal connections to ADC, Operational Amplifier and Comparators
- Two Comparators (CMP):
  - Up to four external inputs

  - Configurable output polarity
  - External output via Peripheral Pin Select
- One Operational Amplifier:
  - 2.3 MHz gain bandwidth
  - Programmable gain
  - Internal gain resistor ladder
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- Two Fixed Voltage References (FVR):
  - Selectable 1.024V, 2.048V and 4.096V output levels
  - FVR1 internally connected to ADC
  - FVR2 internally connected to Comparator and DAC

Clocking Structure

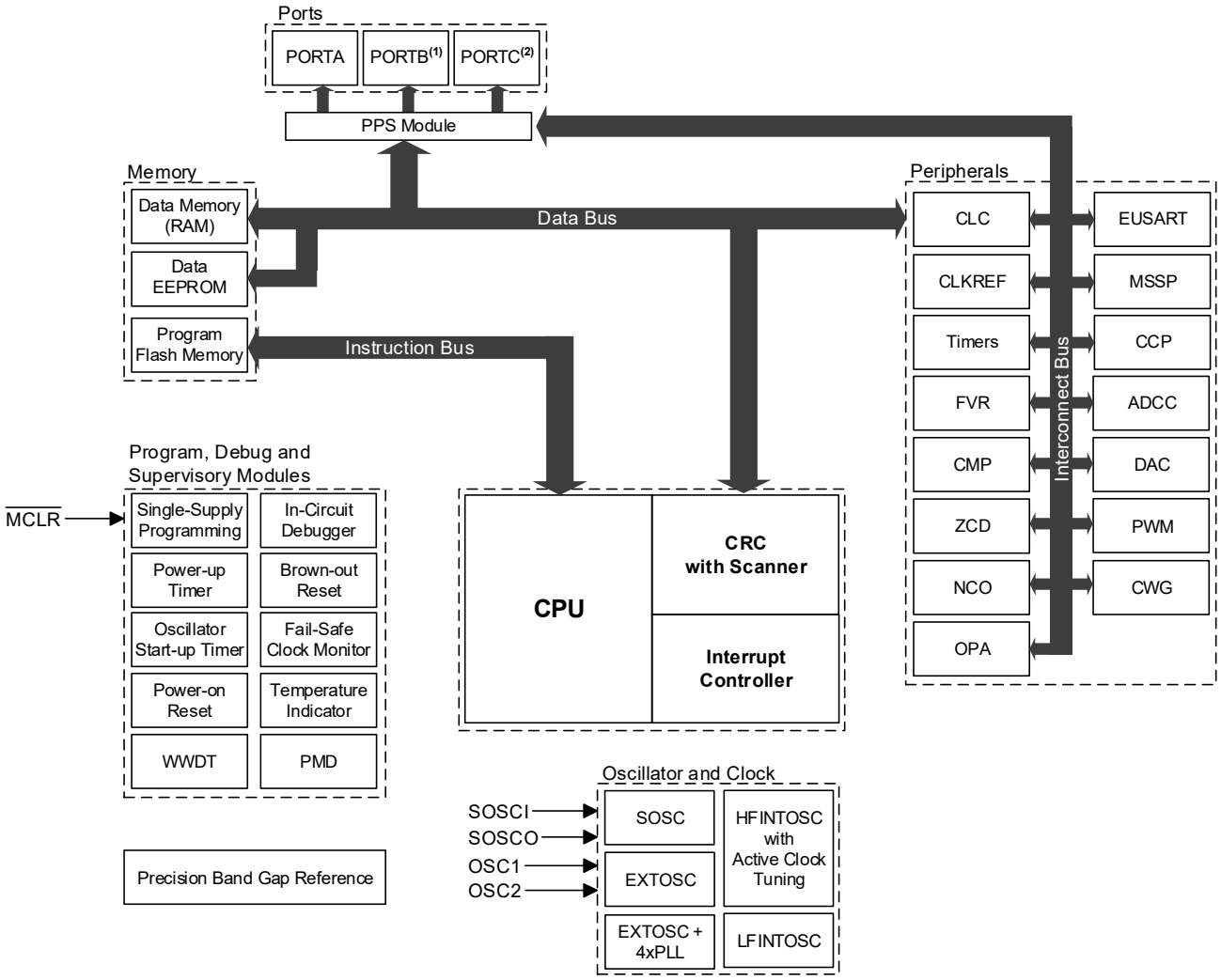
- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 32 MHz
  - ±2% at calibration
  - Active Clock Tuning of HFINTOSC for improved accuracy
- Internal 31 kHz Oscillator (LFINTOSC)
- External 32 kHz Secondary Oscillator (SOSC)
- External High-Frequency Clock Input:
  - Three Crystal/Resonator modes
  - Two External Clock (EC) Power modes
  - 4x PLL available for external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if the external clock source stops
- Oscillator Start-up Timer (OST):
  - Ensures the stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

Block Diagram

Figure 1. PIC16F17114/15/24/25/44/45 Block Diagram



Notes:

1. Available on 20-pin devices only.
2. Available on 14/20-pin devices only.