28-Pin, Low-Power, High-Performance Microcontroller with XLP Technology

PIC18F24/25Q71

www.microchip.com Product Pages: PIC18F24Q71, PIC18F25Q71

Introduction

The PIC18-Q71 microcontroller family is available in 28/40/44/48-pin devices for high bandwidth mixed signal and sensor applications. This is an ideal solution for lighting, motor control and medical market segments. This analog-focused family features a 12-bit Differential ADC with Computation and Context Switching, two Operational Amplifiers, a 10-bit Digital-to-Analog Converter (DAC) and two 8-bit DAC modules with buffered outputs and internal connections to other peripherals, and two advanced high-speed Analog Comparators. This device family also features the Analog Peripheral Manager to manage analog peripherals for optimizing power consumption. The PIC18-Q71 microcontroller family also features the 8-bit Signal Routing Port module to interconnect digital peripherals without using external pins.

PIC18-Q71 Family Types

Table 1. Devices Included in This Data Sheet

Device	Program Memory Flash (Bytes)	Data SRAM (Bytes)	Data EEPROM (Bytes)	Memory Access Partition/ Device Information Area	I/O Pins/ Peripheral Pin Select	8-Bit Timer with HLT/ 16-Bit Timers	16-Bit Dual PWM/ CCP	Complimentary Waveform Generator	16-Bit Universal Timer	Numerically Controlled Oscillator	Configurable Logic Cell	12-Bit Differential ADCC with Context (Channels)	10-Bit DAC/ 8-Bit DAC	Operational Amplifier	High-Speed Comparator/ Zero-Cross Detect	High/Low-Voltage Detect	SPI/I²C	UART/ UART with Protocol Support	Direct Memory Access (DMA)	Windowed Watchdog Timer	Signal Routing Port/ Analog Peripheral Manager	32-Bit CRC with Scanner/ Vectored Interrupts	Peripheral Module Disable	Temperature Indicator
PIC18F24Q71	16K	1024	256	Y/Y	26/Y	2/3	3/2	1	2	1	8	24	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y
PIC18F25Q71	32K	2048	256	Y/Y	26/Y	2/3	3/2	1	2	1	8	24	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y

Table 2. Devices Not Included in This Data Sheet

Device	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins/ Peripheral Pin Select	8-Bit Timer with HLT/ 16-Bit Timers	16-Bit Dual PWM/ CCP	Complimentary Waveform Generator	16-Bit Universal Timer	Numerically Controlled Oscillator	Configurable Logic Cell	12-Bit Differential ADCCC (channels)	10-Bit DAC/ 8-Bit DAC	Operational Amplifier	High-Speed Comparator/ Zero-Cross Detect	High-Low Voltage Detect	SPI/I²C	UART/ UART with Protocol Support	Direct Memory Access (DMA)	Windowed Watchdog Timer	Signal Routing Ports/ Analog Peripheral Manager	32-Bit CRC with Scanner/ Vectored Interrupts	Peripheral Module Disable	Temperature Indicator
PIC18F26Q71	64K	4096	256	Y/Y	26/Y	2/3	3/2	1	2	1	8	24	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y
PIC18F44Q71	16K	1024	256	Y/Y	37/Y	2/3	3/2	1	2	1	8	35	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y
PIC18F45Q71	32K	2048	256	Y/Y	37/Y	2/3	3/2	1	2	1	8	35	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y
PIC18F46Q71	64K	4096	256	Y/Y	37/Y	2/3	3/2	1	2	1	8	35	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y
PIC18F54Q71	16K	1024	256	Y/Y	44/Y	2/3	3/2	1	2	1	8	43	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y
PIC18F55Q71	32K	2048	256	Y/Y	44/Y	2/3	3/2	1	2	1	8	43	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y
PIC18F56Q71	64K	4096	256	Y/Y	44/Y	2/3	3/2	1	2	1	8	43	1/2	2	2/1	1	1/1	1/1	4	Y	Y/Y	Y/Y	Y	Y

Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Four Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either the Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User-programmable source and destination sizes
  - Hardware and software-triggered data transfers
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency of three instruction cycles
  - Programmable vector table base address
  - Backward compatible with previous interrupt capabilities
- 128-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short intervals between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:

  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Memory

- Up to 64 KB of Program Flash Memory
- Up to 4 KB of Data SRAM Memory
- 256 Bytes Data EEPROM
- Memory Access Partition: The Program Flash Memory Can Be Partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Temperature indicator factory calibrated data
  - Fixed Voltage Reference measurement data
  - Microchip Unique Identifier
- Device Characteristics Information (DCI) Area Stores:
  - Program/erase row sizes
  - Pin count details
  - EEPROM size
- Direct, Indirect and Relative Addressing Modes

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (CPU Is Typically Slower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Analog Peripheral Manager:
  - Can be used to optimize power consumption in applications that use analog peripherals by switching them on and off as needed, core independently using dedicated timer resources
- Low-Power Mode Features:
  - Sleep: < 1 µA typical @ 3V
  - Operating Current:
    - 48 µA @ 32 kHz, 3V, typical

Digital Peripherals

- Three 16-Bit Pulse-Width Modulators (PWM):
  - Dual outputs for each PWM module
  - Integrated 16-bit timer/counter
  - Double-buffered user registers for duty cycles
  - Right/Left/Center/Variable Aligned modes of operation
  - Multiple clock and Reset signal selections

- Three 16-Bit Timers (TMR0/1/3)
- Two 8-Bit Timers (TMR2/4) with Hardware Limit Timer (HLT)
- Two Universal Timers (TU16A/TU16B):
  - New Timer modules with features of TMR0/TMR1/TMR2 (Gate, Hardware Limit)
  - Two 16-bit timers can be chained together to create a combined 32-bit timer
- Eight Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- One Complimentary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full Bridge, Half Bridge, One-Channel drive modes
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Two Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- One Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input clock up to 64 MHz
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 32-bit CRC over any portion of Program Flash Memory
- Two UART Modules:
  - One module (UART1) supports LIN host and client, DALI® mode and DMX512 mode
  - Asynchronous UART, RS-232, RS-485 compatible
  - Automatic and user timed BREAK period generation
  - Automatic checksums
  - Programmable Stop bits (1, 1.5 and 2 Stop bits)
  - Wake-up on BREAK reception
  - DMA compatible
- One SPI Module:
  - Configurable length bytes
  - Arbitrary length data packets
  - Transmit-without-receive and receive-without-transmit options
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- One I^2C Module, SMBus, PMBus™ Compatible:
  - Supports Standard mode (100 kHz), Fast mode (400 kHz) and Fast mode plus (1 MHz) modes of operation
  - 7-bit and 10-bit Addressing modes with Address Masking modes
  - Dedicated address, transmit and receive buffers and DMA capabilities

  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I^2C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
  - Multi-Host mode, including self-addressing
- 8-Bit Signal Routing Port Module:
  - Provides internal ports used to interconnect digital peripherals
  - Module can form hardware state machines without any external pins
  - Interrupt-on-change and DMA triggers available on all Signal Routing pins
- Device I/O Port Features:
  - 26 I/O pins (PIC18F24/25/26Q71)
  - 37 I/O pins (PIC18F44/45/46Q71)
  - 44 I/O pins (PIC18F54/55/56Q71)
  - Individually programmable I/O direction, open-drain, slew rate and weak pull-up control
  - Interrupt-on-change on most pins
  - Three programmable external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Analog Peripherals

- Differential Analog-to-Digital Converter with Computation and Context Switching:
  - Up to 43 external channels
  - Up to 140 ksps
  - Differential or single-ended ADC conversion
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - Four Separate Contexts (settings and results) saved and accessible separately
  - Contexts can be accessed through firmware or DMA
  - Operates in Sleep
  - Nine internal analog channels
  - Hardware Capacitive Voltage Divider (CVD) support:
    - Adjustable Sample-and-Hold capacitor array
    - Guard ring digital output drive
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
- One 10-Bit Digital-to-Analog Converters (DAC):
  - Buffered output available on two I/O pins
  - Internal connections to ADC and Comparators
- Two 8-Bit Digital-to-Analog Converters (DAC):
  - Buffered output available on two I/O pins
  - Internal connections to ADC, OPA and Comparators
- Two High-Speed Comparators (CMP):

  - High-Speed mode and Low-Power modes available
  - Four external inputs
  - Configurable output polarity
  - External output via Peripheral Pin Select
- Two Operational Amplifiers:
  - 5.5 MHz Gain Bandwidth
  - Programmable Gain using Internal Resistor Ladder
  - Built-in hardware peak detect operation
  - Automatic input offset voltage calibration
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
  - Internal connections to ADC, Comparator and DAC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - ±1% at calibration
  - Active Clock Tuning of HFINTOSC for better accuracy
- 31 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-Frequency Oscillator Block:
  - Three crystal/resonator modes
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if external clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

PIC18-Q71 Block Diagram