PIC16F17524/25/44/45 Full-Featured 14/20-Pin Microcontrollers

PIC16F17524/25/44/45

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Introduction

The PIC16F17576 microcontroller family, with its analog focused set of peripherals, provides an effective single device method of implementing mixed signal and sensor solutions.

This family is available in a wide variety of packages from 14 to 44 pins, and offers up to 28 KB of Program Flash Memory with up to 2 KB of RAM and up to 256 bytes of Data Flash Memory (EEPROM). Included in the analog peripherals is a 12-bit Differential Analog to Digital Converter with Computation (ADCC) capable of up to 300 ksps, two 10-bit Digital to Analog Converters (DAC), up to four Operational Amplifiers (OPA), and two Comparators. This device family also features an Analog Peripheral Manager (APM) to switch analog peripherals on/off for optimized power consumption, while a low-power voltage reference provides a highly accurate voltage reference across operating voltages and temperature ranges. Among the digital features of the family is the 8-bit Signal Routing Port (SRP) module, which offers the ability to interconnect digital peripherals without using external pins. In addition, there is a collection of other peripherals including timing control, basic logic operations, and serial communications.

Small form-factored robust packaging options, combined with a tailored set of Core Independent Peripherals, makes the PIC16F17576 family well-suited for a variety of applications across market segments from real-time control to digital sensor nodes.

PIC16F17576 Family Summary

Table 1. Devices Included in This Data Sheet

Device	Program Flash Memory (bytes)	Data SRAM (bytes)	Data Flash Memory (EEPROM) (bytes)	Memory Access Partition/ Device Information Area	I/O Pins(1)/ SRPORT Pins	8-Bit Timers with HLT/ 16-Bit Timers(2)	16-Bit PWM/ CCP	12-Bit ADC Channels (External+/External-/Internal)	I2C/SPI	EUSART	NCO	CWG	CLC	FVR	CMP/CMP(LP)	10-bit DAC	Operational Amplifier	ZCD	SMBus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Windowed Watchdog Timer
PIC16F17524	7K	512	128	Y/Y	12/8	2/2	2/2	11/11/7	2/2	2	1	1	4	2	1/1	2	1	1	Y	1	12	Y
PIC16F17525	14K	1024	128	Y/Y	12/8	2/2	2/2	11/11/7	2/2	2	1	1	4	2	1/1	2	1	1	Y	1	12	Y
PIC16F17544	7K	512	128	Y/Y	18/8	2/2	2/2	17/17/7	2/2	2	1	1	4	2	1/1	2	1	1	Y	1	18	Y
PIC16F17545	14K	1024	128	Y/Y	18/8	2/2	2/2	17/17/7	2/2	2	1	1	4	2	1/1	2	1	1	Y	1	18	Y

Table 2. Devices Not Included in This Data Sheet

Device	Program Flash Memory (bytes)	Data SRAM (bytes)	Data Flash Memory (EEPROM) (bytes)	Memory Access Partition/ Device Information Area	I/O Pins(1)/ SRPORT Pins	8-Bit Timers with HLT/ 16-Bit Timers(2)	16-Bit PWM/ CCP	12-Bit ADC Channels (External+/External-/Internal)	I2C/SPI	EUSART	NCO	CWG	CLC	FVR	CMP/CMP(LP)	10-bit DAC	Operational Amplifier	ZCD	SMBus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Watchdog Timer
PIC16F17526	28K	2048	256	Y/Y	12/8	2/2	2/2	11/11/7	2/2	2	1	1	4	2	1/1	2	1	1	Y	1	12	Y
PIC16F17546	28K	2048	256	Y/Y	18/8	2/2	2/2	17/17/7	2/2	2	1	1	4	2	1/1	2	1	1	Y	1	18	Y
PIC16F17554	7K	512	128	Y/Y	25/8	3/2	2/2	24/11/7	2/2	2	1	1	4	2	1/1	2	3	1	Y	1	25	Y
PIC16F17555	14K	1024	128	Y/Y	25/8	3/2	2/2	24/11/7	2/2	2	1	1	4	2	1/1	2	3	1	Y	1	25	Y
PIC16F17556	28K	2048	256	Y/Y	25/8	3/2	2/2	24/11/7	2/2	2	1	1	4	2	1/1	2	3	1	Y	1	25	Y
PIC16F17574	7K	512	128	Y/Y	36/8	3/2	2/2	35/16/7	2/2	2	1	1	4	2	1/1	2	4	1	Y	1	25	Y
PIC16F17575	14K	1024	128	Y/Y	36/8	3/2	2/2	35/16/7	2/2	2	1	1	4	2	1/1	2	4	1	Y	1	25	Y
PIC16F17576	28K	2048	256	Y/Y	36/8	3/2	2/2	35/16/7	2/2	2	1	1	4	2	1/1	2	4	1	Y	1	25	Y

Notes:

1. Total I/O count includes one pin ($\overline{\text{MCLR}}$) that is input-only.
2. Timer0 can be configured as either an 8-bit or 16-bit timer.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC-32 MHz clock input
  - 125 ns minimum instruction time
- 16-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power Brown-out Reset (LPBOR)
- Windowed Watchdog Timer (WWDT)

Memory

- Up to 28 KB of Program Flash Memory
- Up to 2 KB of Data SRAM Memory
- Up to 256 Bytes of Data EEPROM Memory
- Memory Access Partition (MAP) with Program Flash Memory Partitioned into:
  - Application block
  - Boot block
  - Storage Area Flash (SAF) block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:

  - Fixed Voltage Reference (FVR) measurement data
  - Microchip Unique Identifier (MUI)
- Device Characteristics Information (DCI) Stores:
  - Program/erase row sizes
  - Pin count details
- Direct, Indirect, and Relative Addressing Modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep:
  - Lowest power consumption
  - Reduced system electrical noise while performing ADC conversions
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware modules to minimize active power consumption of unused peripherals
- Analog Peripheral Manager:
  - Can be used to optimize power consumption in applications that use analog peripherals by switching them on and off as needed, core independently using dedicated timer resources
- Low Power Mode Features:
  - Sleep:
    - < 900 nA typical @ 3V/25°C (WDT enabled)
    - < 600 nA typical @ 3V/25°C (WDT disabled)
  - Operating Current:
    - 48 µA typical @ 32 kHz, 3V/25°C
    - < 1 mA typical @ 4 MHz, 5V/25°C

Digital Peripherals

- Two Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Two Pulse-Width Modulators (PWM):
  - 16-bit resolution
  - Independent pulse outputs
  - ERS inputs
- Four Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic

- One Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, one-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- One Configurable 8/16-Bit Timer (TMR0)
- Two 16-Bit Timers (TMR1/3) with Gate Control
- Up to Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- One Numerically Controlled Oscillator
  - Generates true linear frequency control and increased frequency resolution
  - Input clock up to 64 MHz
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 32-bit CRC over any portion of Program Flash Memory
- Two Enhanced Universal Synchronous Asynchronous Receiver Transmitters (EUSART):
  - RS-232, RS-485, LIN compatible
  - Auto-wake-up on Start
- Two Host Synchronous Serial Ports (MSSP):
  - Serial Peripheral Interface (SPI) mode
    - Chip Select Synchronization
  - Inter-Integrated Circuit (I^2C) mode
    - 7/10-bit Addressing modes
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Device I/O Port Features:
  - Up to 35 I/O pins
  - One input-only pin
  - Individual I/O direction, open-drain, input threshold, slew rate and weak pull-up control
  - Interrupt-on-Change (IOC) on up to 25 pins
  - One External Interrupt pin

Analog Peripherals

- Differential Analog-to-Digital Converter with Computation (ADCC):
  - Sample rate up to 300 ksps
  - 12-bit resolution
  - Up to 35 external input channels
  - Seven internal input channels
  - Internal ADC oscillator (ADCRC)
  - Operates in Sleep
  - Selectable auto-conversion trigger sources
- Two 10-Bit Digital-to-Analog Converters (DAC):

  - Buffered output available on up to two I/O pins
  - Internal connections to ADC, Op Amps, and Comparators
- Two Comparators (CMP):
  - One High-Speed Comparator (CMP1):
    - Configurable power modes for faster response time (50ns) or lower power operation
    - Multiple hysteresis selections
    - Up to four external inputs
    - Configurable output polarity
    - External output via Peripheral Pin Select
  - One Low-Power Comparator (CMPLP1):
    - Selectable Input Common Mode ranges, including rail-to-rail
    - Low operating current
    - Up to four external inputs
    - Configurable output polarity
    - External output via Peripheral Pin Select
- Up to Four Operational Amplifiers:
  - Programmable Gain using Internal Resistor Ladder
  - Automatic input offset voltage calibration
- Two Fixed Voltage References (FVR):
  - Selectable 1.024V, 2.048V and 4.096V output levels
  - FVR1 internally connected to ADC
  - FVR2 internally connected to Comparator and DAC
- Low Power Voltage Reference (VREFLP)
  - Nominal 1.024V output
  - Independent 6-bit DAC

Clocking Structure

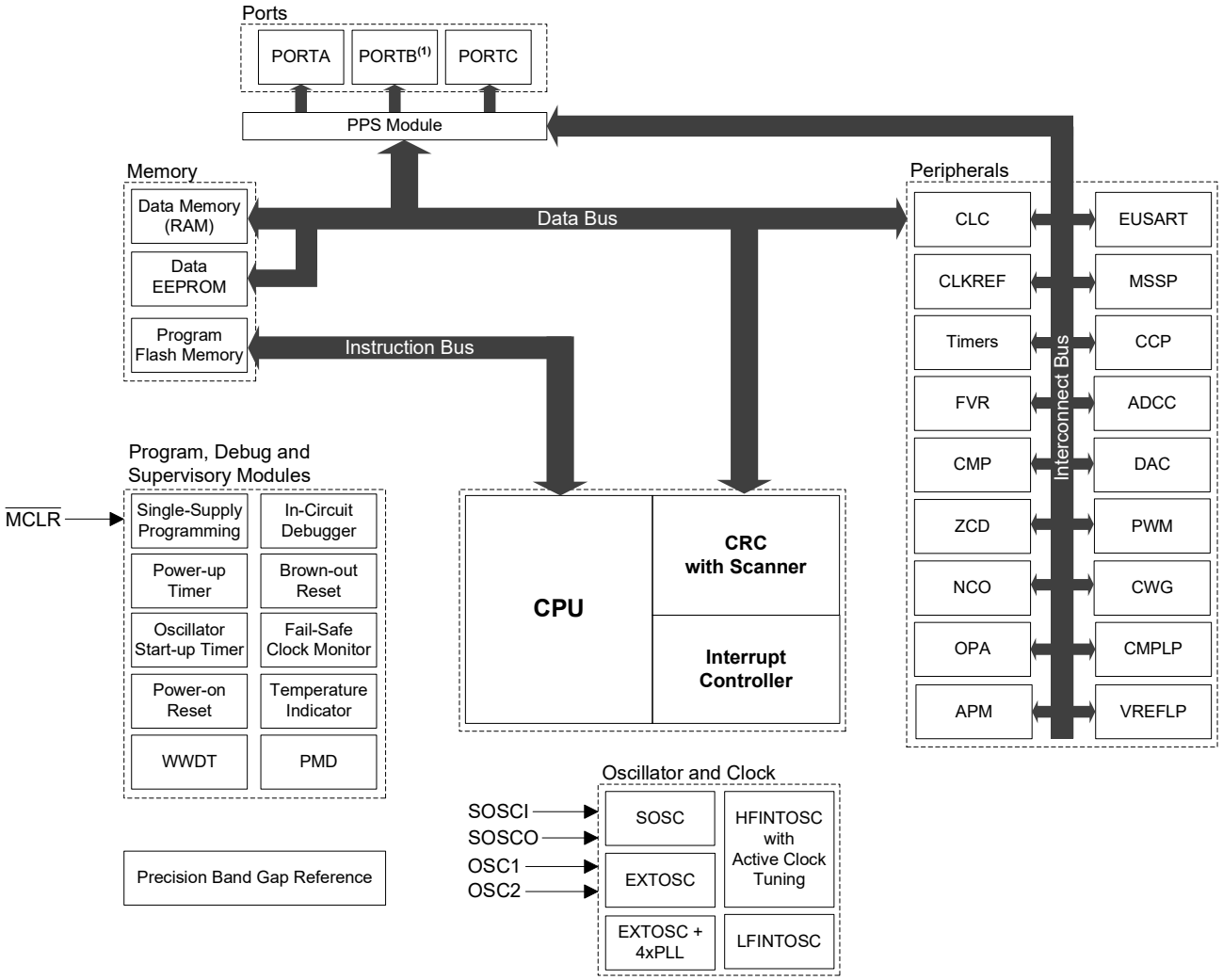
- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 32 MHz
  - ±2% at calibration
  - Active Clock Tuning of HFINTOSC for improved accuracy
- Internal 31 kHz Oscillator (LFINTOSC)
- External 32 kHz Secondary Oscillator (SOSC)
- External High-Frequency Clock Input:
  - Three Crystal/Resonator modes
  - Two External Clock (EC) Power modes
  - 4xPLL available for external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if the external clock source stops
- Oscillator Start-up Timer (OST):
  - Ensures the stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

Block Diagram

Figure 1. PIC16F17526/46 Block Diagram



Note:

1. Available on 40-pin devices only.