28/40/44/48-Pin, Low-Power, High-Performance Microcontroller with XLP Technology

PIC18F26/46/56Q83

Introduction

The PIC18-Q83 microcontroller family is available in 28/40/44/48-pin devices for many automotive and industrial applications. The many communication peripherals found in the product family, such as Controller Area Network (CAN), Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I^2C), and two Universal Asynchronous Receiver Transmitters (UARTs), can handle a wide range of wired and wireless (using external modules) communication protocols for intelligent applications. Combined with the Core Independent Peripherals (CIPs) integration capabilities, this capacity enables functions for motor control, power supply, sensor, signal and user interface applications. Additionally, this family includes a 12-bit Analog-to-Digital Converter (ADC) with Computation and Context Switching extensions for automated signal analysis to reduce the complexity of the application.

PIC18-Q83 Family Types

Table 1. Devices Included in This Data Sheet

Device	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins/ Peripheral Pin Select	8-Bit Timer with HLT/ 16-Bit Timers	16-Bit Dual PWM/ CCP	Complimentary Waveform Generator	Signal Measurement Timer	16-Bit Universal Timer	Numerically Controlled Oscillator	Configurable Logic Cell	12-Bit ADC w/Computation and Context Switching (channels)	8-Bit DAC	Comparator/ Zero-Cross Detect	High/Low-Voltage Detect	CAN	SPI/I^2C	UART/ UART with Protocol Support	Direct Memory Access (DMA)	Windowed Watchdog Timer	32-Bit CRC with Scanner	Vectored Interrupts	Peripheral Module Disable	Temperature Indicator	JTAG Boundary Scan
PIC18F26Q83	64k	8192	1024	Y/Y	25/Y	3/3	4/3	3	1	2	3	8	24	1	2/1	1	Y	2/1	3/2	8	Y	Y	Y	Y	Y	Y
PIC18F46Q83	64k	8192	1024	Y/Y	36/Y	3/3	4/3	3	1	2	3	8	35	1	2/1	1	Y	2/1	3/2	8	Y	Y	Y	Y	Y	Y
PIC18F56Q83	64k	8192	1024	Y/Y	44/Y	3/3	4/3	3	1	2	3	8	43	1	2/1	1	Y	2/1	3/2	8	Y	Y	Y	Y	Y	Y

Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Eight Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces

  - User-programmable source and destination sizes
  - Hardware and software triggered data transfers
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency of three instruction cycles
  - Programmable vector table base address
  - Backward compatible with previous interrupt capabilities
- 128-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short interval between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection

Memory

- Up to 128 KB of Program Flash Memory
- Up to 13 KB of Data SRAM Memory
- 1024 Bytes Data EEPROM
- Memory Access Partition: The Program Flash Memory Can Be Partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Temperature indicator factory calibrated data
  - Fixed Voltage Reference measurement data
  - Microchip Unique Identifier
- Device Characteristics Information (DCI) Area Stores:
  - Program/erase row sizes
  - Pin count details
  - EEPROM size
- Direct, Indirect, and Relative Addressing Modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (Typically CPU Is Lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Low-Power Mode Features:
  - Sleep: < 1 µA typical @ 3V
  - Operating current:
    - 48 µA @ 32 kHz, 3V, typical

Digital Peripherals

- Four 16-Bit Pulse-Width Modulators (PWM):
  - Dual outputs for each PWM module
  - Integrated 16-bit timer/counter
  - Double-buffered user registers for duty cycles
  - Right/Left/Center/Variable Aligned modes of operation
  - Multiple clock and Reset signal selections
- Three 16-Bit Timers (TMR0/1/3)
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Two Universal Timers (TMRU16A/16B):
  - New Timer modules with features of TMR0/TMR1/TMR2 (Gate, Hardware Limit)
  - Two 16-bit timers can be chained together to create a combined 32-bit timer
- Eight Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Three Complimentary Waveform Generators (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Three Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Three Numerically Controlled Oscillators (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input clock up to 64 MHz
- Signal Measurement Timer (SMT):
  - 24-bit timer/counter with prescaler
  - Several modes of operation such as Time-of-Flight, Period and Duty Cycle measurement, etc.
- Data Signal Modulator (DSM):

  - Multiplex two carrier clocks, with glitch prevention feature
  - Multiple sources for each carrier
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 16-bit CRC over any portion of Program Flash Memory
- CAN Module:
  - Full CAN 2.0B compatibility
  - One dedicated transmit FIFO
  - Three programmable transmit/receive FIFOs
  - One transmit event queue
  - 12 acceptance masks/filters
- Five UART Modules:
  - LIN host and client, DMX mode, DALI gear and device protocols
  - Asynchronous UART, RS-232, RS-485 compatible
  - Automatic and user timed BREAK period generation
  - Automatic checksums
  - Programmable 1, 1.5, and two Stop bits
  - Wake-up on BREAK reception
  - DMA compatible
- Two SPI Modules:
  - Configurable length bytes
  - Arbitrary length data packets
  - Transmit-without-receive and receive-without-transmit options
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- One I^2C module, SMBus, PMBus™ Compatible:
  - 7-bit and 10-bit Addressing modes with Address Masking modes
  - Dedicated address, transmit and receive buffers and DMA capabilities
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I^2C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Multi-Host mode, including self-addressing
- Device I/O Port Features:
  - 25 I/O pins (PIC18F26/27Q83)
  - 36 I/O pins (PIC18F46/47Q83)
  - 44 I/O pins (PIC18F56/57Q83)
  - Individually programmable I/O direction, open-drain, slew rate and weak pull-up control
  - Interrupt-on-change on most pins
  - Three programmable external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Analog Peripherals

- Analog-to-Digital Converter with Computation and Context Switching:
  - Up to 43 external channels
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - Four Separate Contexts (settings and results) saved and accessible separately
  - Contexts can be accessed through firmware or DMA
  - Operates in Sleep
  - Five internal analog channels
  - Hardware Capacitive Voltage Divider (CVD) Support:
    - Adjustable sample and hold capacitor array
    - Guard ring digital output drive
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
- 8-Bit Digital-to-Analog Converter (DAC):
  - Buffered output available on two I/O pins
  - Internal connections to ADC and Comparators
- Two Comparators (CMP):
  - Four external inputs
  - Configurable output polarity
  - External output via Peripheral Pin Select
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
  - Internal connections to ADC, Comparator and DAC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - ±1% at calibration
  - Active Clock Tuning of HFINTOSC for better accuracy
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-Frequency Oscillator Block:
  - Three crystal/resonator modes
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if external clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip