28-Pin, Low-Power, High-Performance Microcontroller with XLP Technology

PIC18F24/25Q24

Product Page Links

Introduction

The PIC18-Q24 microcontroller family is available in 28/40/44/48-pin devices for sensor-interfacing, real-time control and communication applications. The family showcases a Multi-Voltage I/O (MVIO) interface with multiple pins I/O powered by an alternative V_{DD} pin, allowing these pins to operate at a different voltage domain than the rest of the microcontroller. This family also features a 10-bit Analog-to-Digital Converter with Computation (ADCC) capable of 300 ksps and the 8-bit Signal Routing Port module to interconnect digital peripherals without using external pins.

Additionally, the PIC18-Q24 microcontroller family offers Enhanced Code Protection features that can be used to provide increased security and protection of user firmware and data. These Enhanced Code Protection features include the ability to disable the programming and debugging interface to allow for one time device programmability and effectively block any unauthorized attempts to communicate with the device via the ICSP™ interface.

Additional features include vectored interrupt controller with fixed latency for handling interrupts; system bus arbiter; Direct Memory Access (DMA) capabilities; Universal Asynchronous Receiver-Transmitter (UART) with support for asynchronous, DMX-512, Digital Addressable Lighting Interface (DALI®) and Local Interconnect Network (LIN) protocols; Serial Peripheral Interface (SPI); and I^2C. This family also includes memory features such as Memory Access Partition (MAP) and the Device Information Area (DIA) which stores factory calibration values to help improve temperature sensor accuracy.

PIC18-Q24 Family Types

Table 1. Memory Overview

Devices	PIC18F24Q24	PIC18F25Q24 PIC18F45Q24 PIC18F55Q24	PIC18F26Q24 PIC18F46Q24 PIC18F56Q24
Program Flash Memory	16 KB	32 KB	64 KB
Data SRAM	1 KB	2 KB	4 KB
Data EEPROM	512B	512B	512B
Memory Access Partition (MAP)	Yes	Yes	Yes
Device Information Area (DIA)	Yes	Yes	Yes
Programming and Debugging Interface Disable (PDID)	Yes	Yes	Yes

Table 2. Peripheral Overview

Feature	PIC18F24Q24 PIC18F25Q24 PIC18F26Q24	PIC18F45Q24 PIC18F46Q24	PIC18F55Q24 PIC18F56Q24
Pins	28	40	48

Table 2. Peripheral Overview (continued)

Feature	PIC18F24Q24 PIC18F25Q24 PIC18F26Q24	PIC18F45Q24 PIC18F46Q24	PIC18F55Q24 PIC18F56Q24
I/O Pins	24	35	43
Peripheral Pin Select (PPS)	Yes	Yes	Yes
Multi-Voltage I/O (MVIO) Pins	4 (on V_{DDIO2})	12 (on V_{DDIO2})	12 (on V_{DDIO2})
High-Voltage Tolerant Pins	4	12	12
Signal Routing Port (8-Pin)	1	1	1
8-Bit Timer with HLT (TMR2)	3	3	3
16-Bit Timers (TMR0/1)	3	3	3
16-Bit Universal Timer (UTMR)	2	2	2
16-Bit Dual PWM	3	3	3
Capture/Compare/PWM (CCP)	2	2	2
Complementary Waveform Generator (CWG)	1	1	1
Configurable Logic Cell (CLC)	8	8	8
10-Bit Analog-to-Digital Converter with Computation (ADCC) External Channels	19	22	30
High/Low-Voltage Detect (HLVD)	1	1	1
High-Speed Analog Comparator (CMP)	2	2	2
Zero-Cross Detect (ZCD)	2	2	2
8-Bit Digital-to-Analog Converter (DAC)	1	1	1
Serial Peripheral Interface (SPI)	2	2	2
Inter-Integrated Circuit (I^2C)	2	2	2
Universal Asynchronous Receiver Transmitter (UART)	1	1	1
UART with Protocol Support	1	1	1
Direct Memory Access (DMA) Channels	4	4	4
Windowed Watchdog Timer (WWDT)	Yes	Yes	Yes
32-Bit CRC with Scanner	Yes	Yes	Yes
Vectored Interrupts	Yes	Yes	Yes
Interrupt-on-Change (IOC)	Yes	Yes	Yes
Peripheral Module Disable (PMD)	Yes	Yes	Yes
Temperature Indicator	Yes	Yes	Yes

Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Multi-Voltage I/O (MVIO):
  - Allows for operation at a voltage domain different than the normal microcontroller operating voltage
  - Provides multiple I/O pins powered by the V_{DDIO2} voltage domain
  - Dedicated Low-Voltage Detect circuitry and interrupt for V_{DDIO2} domain
  - MVIO pins support a voltage range of 1.62V through 5.5V
- Four Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either the Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User-programmable source and destination sizes
  - Hardware and software-triggered data transfers
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency of three instruction cycles
  - Programmable vector table base address
  - Backward compatible with previous interrupt capabilities
- 128-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short intervals between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection

Operating Characteristics

- Operating Voltage Range (V_{DD}):
  - 1.8V to 5.5V
- Multi-Voltage I/O (MVIO) Range (V_{DDIO2}):
  - 1.62V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Memory

- Up to 64 KB of Program Flash Memory
- Up to 4 KB of Data SRAM Memory

- 512 Bytes Data EEPROM
- Memory Access Partition: The Program Flash Memory Can Be Partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block
- Programmable Code Protection and Write Protection
- Enhanced Code Protection
  - Programming and Debugging Interface Disable (PDID) through the $\overline{\text{ICSPDIS}}$ Configuration bit
  - Storage Area Flash (SAF) one-time programmability through the $\overline{\text{SAFLOCK}}$ Configuration bit
- Device Information Area (DIA) Stores:
  - Temperature indicator factory calibrated data
  - Fixed Voltage Reference measurement data
  - Microchip Unique Identifier
- Device Characteristics Information (DCI) Area Stores:
  - Program/erase row sizes
  - Pin count details
  - EEPROM size
- Direct, Indirect and Relative Addressing Modes

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (CPU Is Typically Slower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Low Power Mode Features:
  - Sleep: < 1 µA typical @ 3V
  - Operating Current: 48 µA @ 32 kHz, 3V, typical

Digital Peripherals

- Three 16-Bit Pulse-Width Modulators (PWM):
  - Dual outputs for each PWM module
  - Integrated 16-bit timer/counter
  - Double-buffered user registers for duty cycles
  - Right/Left/Center/Variable Aligned modes of operation
  - Multiple clock and Reset signal selections
- Three 16-Bit Timers (TMR0/1/3)
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Two Universal Timers (TU16A/TU16B):
  - New Timer module that combines most of the operations of all legacy timers (TMR0/1/2, SMT, CCP) into one single timer
  - Two 16-bit timers can be chained together to create a combined 32-bit timer

- Eight Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- One Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full Bridge, Half Bridge, One-Channel drive modes
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Two Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- One Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input clock up to 64 MHz
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 32-bit CRC over any portion of Program Flash Memory
- Two UART Modules:
  - One module (UART1) supports LIN host and client, DALI® mode and DMX mode
  - Asynchronous UART, RS-232, RS-485 compatible
  - Automatic and user timed BREAK period generation
  - Automatic checksums
  - Programmable Stop bits (1, 1.5 and 2 Stop bits)
  - Wake-up on BREAK reception
  - DMA compatible
- Two SPI Modules:
  - Configurable length bytes
  - Arbitrary length data packets
  - Transmit-without-receive and receive-without-transmit options
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- Two I^2C Modules, SMBus, PMBus™ Compatible:
  - Supports Standard mode (100 kHz), Fast mode (400 kHz) and Fast mode plus (1 MHz) modes of operation, with built-in internal pull-up resistors
  - 7-bit and 10-bit Addressing modes with Address Masking modes
  - Dedicated address, transmit and receive buffers and DMA capabilities
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I^2C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
  - Multi-Host mode, including self-addressing

- One 8-Bit Signal Routing Port Module:
  - Eight signal routing pins per module
  - Supports software read/write and customizable input/output control
  - Supports flip-flops and clock source selection for Hardware State Machine and shift register application
  - Integration with PPS, Interrupt-on-Change and DMA/ADC triggers available
- Device I/O Port Features:
  - 24 I/O pins including four MVIO pins powered by V_{DDIO2} (PIC18F24/25/26Q24)
  - 35 I/O pins including 12 MVIO pins powered by V_{DDIO2} (PIC18F45/46Q24)
  - 43 I/O pins including 12 MVIO pins powered by V_{DDIO2} (PIC18F55/56Q24)
  - MVIO pins support a voltage range of 1.62V through 5.5V
  - Individually programmable I/O direction, open-drain, slew rate, and weak pull-up control
  - Low-voltage interface on all I/O pins using LV-TTL input buffer
  - Interrupt-on-change on most pins
  - Three programmable external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Analog Peripherals

- 10-Bit Analog-to-Digital Converter with Computation (ADCC):
  - Up to 30 external channels
  - Up to 300 ksps
  - Supports grouping of external channels
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Nine internal analog channels
  - Hardware Capacitive Voltage Divider (CVD) support:
    - Adjustable Sample-and-Hold capacitor array
    - Guard ring digital output drive
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
- One 8-Bit Digital-to-Analog Converters (DAC):
  - Buffered output available on two I/O pins
  - Internal connections to ADC and Comparators
- Two High-Speed Comparators (CMP):
  - High-Speed mode and Low-Power modes available
  - Four external inputs
  - Configurable output polarity
  - External output via Peripheral Pin Select
- Two Zero-Cross Detect (ZCD) Modules:
  - Detect when AC signal on pin crosses ground
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

  - Internal connections to ADC, Comparator and DAC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - ±1% at calibration
  - Active Clock Tuning of HFINTOSC for better accuracy
- 31 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-Frequency Oscillator Block:
  - Three crystal/resonator modes with configurable HS Crystal mode up to 32 MHz
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if external clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip
- Programming and Debugging Interface Disable (PDID)

PIC18-Q24 Block Diagram