

# 14/20-Pin, Low-Power, High-Performance Microcontroller with XLP Technology

## PIC18F04/05/14/15Q20



## Introduction

The PIC18-Q20 microcontroller family is one of the smallest PIC18 product families available in 14/20-pin devices for sensor-interfacing, real-time control and communication applications.

This family showcases the Improved Inter-Integrated Circuit® (I3C) Target module with a higher communication rate and a 10-bit 300 ksps ADC with Computation for responsive sensor designs. The family features a Multi-Voltage I/O (MVIO) interface with multiple pins powered by  $V_{DDIO2}$  and  $V_{DDIO3}$  that allows for these pins to operate at a different voltage domain than the rest of the microcontroller. The family also features the 8-bit Signal Routing Port module to interconnect digital peripherals without using external pins.

Additional features include vectored interrupt controller with fixed latency for handling interrupts; a system bus arbiter; Direct Memory Access (DMA) capabilities; two UART with support for asynchronous modes and (for the Full-Featured UART) DMX and DALI® lighting control standards and LIN protocol; individual SPI and I<sup>2</sup>C modules; and a programmable 32-bit CRC with memory scan.

This family also includes Memory Access Partition (MAP) featuring a user-configurable Storage Area Flash (SAF) with One-Time Programmability to support users in bootloader applications. Also included is a separate Device Information Area (DIA) to store factory calibration values, to help improve temperature sensor accuracy.

## PIC18-Q20 Family Types

**Table 1.** Memory Overview

Devices	PIC18F04Q20	PIC18F05Q20	PIC18F06Q20
	PIC18F14Q20	PIC18F15Q20	PIC18F16Q20
Program Flash Memory	16 KB	32 KB	64 KB
Data SRAM	1 KB	2 KB	4 KB
Data EEPROM	256B	256B	256B
Memory Access Partition (MAP)	Yes	Yes	Yes
Device Information Area (DIA)	Yes	Yes	Yes

**Table 2.** Peripheral Overview

Feature	PIC18F04Q20	PIC18F14Q20
	PIC18F05Q20	PIC18F15Q20
	PIC18F06Q20	PIC18F16Q20
Pins	14	20
I/O Pins	11	16
Peripheral Pin Select (PPS)	Yes	Yes
Multi-Voltage I/O (MVIO) Pins	2 (on $V_{DDIO2}$ )	4 (2 on $V_{DDIO2}$ and $V_{DDIO3}$ each)
High-Voltage Tolerant Pins	2	4
Signal Routing Port (8-Pin)	1	1
8-Bit Timer with HLT (TMR2)	2	2
16-Bit Timers (TMR0/1)	2	2
16-Bit Universal Timer (UTMR)	2	2

.....continued

Feature	PIC18F04Q20	PIC18F14Q20
	PIC18F05Q20	PIC18F15Q20
	PIC18F06Q20	PIC18F16Q20
16-Bit Dual PWM	2	2
Capture/Compare/PWM (CCP)	2	2
Complementary Waveform Generator (CWG)	1	1
Configurable Logic Cell (CLC)	4	4
10-Bit Analog-to-Digital Converter with Computation (ADCC) External Channels	8	11
High/Low-Voltage Detect (HLVD)	1	1
Serial Peripheral Interface (SPI)	1	1
Inter-Integrated Circuit (I <sup>2</sup> C)	1 Host, up to 2 Clients <sup>(1)</sup>	1 Host, up to 3 Clients <sup>(1)</sup>
Improved Inter-Integrated Circuit (I3C <sup>®</sup> )	1 Target	2 Targets
Universal Asynchronous Receiver Transmitter (UART)	1	1
UART with Protocol Support	1	1
Direct Memory Access (DMA) Channels	4	4
Windowed Watchdog Timer (WWDT)	Yes	Yes
32-Bit CRC with Scanner	Yes	Yes
Vectored Interrupts	Yes	Yes
Interrupt-on-Change (IOC)	Yes	Yes
Peripheral Module Disable (PMD)	Yes	Yes
Temperature Indicator	Yes	Yes

**Note:**

1. The I3C Target module can be configured to operate as an I<sup>2</sup>C Client module when the device is connected to an I<sup>2</sup>C Bus with no I3C Controllers.

## Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Four Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User-programmable source and destination sizes
  - Hardware and software-triggered data transfers
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency of three instruction cycles
  - Programmable vector table base address
  - Backwards compatible with previous interrupt capabilities
- 128-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short interval between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection

## Operating Characteristics

- Operating Voltage Range ( $V_{DD}$ ):
  - 1.8V to 5.5V
- Multi-Voltage I/O (MVIO) Range ( $V_{DDIO2}$  and  $V_{DDIO3}$ ):
  - 1.62V to 5.5V (3.63V with I3C enabled)
  - High-Voltage tolerant MVIO-powered pins support I3C communication down to 0.95V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

## Memory

- Up to 64 KB of Program Flash Memory
- Up to 4 KB of Data SRAM Memory
- 256 Bytes Data EEPROM
- Memory Access Partition: The Program Flash Memory Can Be Partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block

- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Temperature indicator factory calibrated data
  - Fixed Voltage Reference (FVR) measurement data
  - Microchip Unique Identifier
- Device Characteristics Information (DCI) Area Stores:
  - Program/erase row sizes
  - Pin count details
  - EEPROM size
- Direct, Indirect and Relative Addressing Modes

### Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (CPU Is Typically Slower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Low-Power Mode Features:
  - Sleep: < 1  $\mu$ A typical @ 3V
  - Operating Current:
    - 48  $\mu$ A @ 32 kHz, 3V, typical

### Digital Peripherals

- Two 16-Bit Pulse-Width Modulators (PWM):
  - Dual outputs for each PWM module
  - Integrated 16-bit timer/counter
  - Double-buffered user registers for duty cycles
  - Right/Left/Center/Variable Aligned modes of operation
  - Multiple clock and Reset signal selections
- Two 16-Bit Timers (TMR0/1)
- Two 8-Bit Timers (TMR2/4) with Hardware Limit Timer (HLT)
- Two 16-Bit Universal Timers (TU16A/16B):
  - New Timer module that combines most of the operations of all legacy timers (TMR0/1/2, SMT, CCP) into one single timer
  - Two 16-bit timers can be chained together to create a combined 32-bit timer
- Four Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- One Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, one-channel drive
  - Multiple signal sources
  - Programmable dead band

- Fault-shutdown input
- Two Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 32-bit CRC over any portion of Program Flash Memory
- Two UART Modules:
  - One module (UART1) supports LIN host and client, DMX mode, DALI gear and device protocols
  - Asynchronous UART, RS-232, RS-485 compatible
  - Automatic and user timed BREAK period generation
  - Automatic checksums
  - Programmable Stop bits (1, 1.5 and 2 Stop bits)
  - Wake-up on BREAK reception
  - DMA compatible
- One SPI Module:
  - Configurable length bytes
  - Arbitrary length data packets
  - Transmit-without-receive and receive-without-transmit options
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- One I<sup>2</sup>C Module, SMBus, PMBus™ Compatible:
  - Supports Standard mode (100 kHz), Fast mode (400 kHz) and Fast mode Plus (1 MHz) modes of operation
  - 7-bit and 10-bit Addressing modes with Address Masking modes
  - Dedicated address, transmit and receive buffers and DMA capabilities
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I<sup>2</sup>C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
  - Multi-Host mode, including self-addressing
  - Built-in Error Detection and Recovery
- Up To Two I3C Modules:
  - Supports I3C target device mode only
  - Can be used as an I<sup>2</sup>C Client module
  - Adheres to MIPI I3C Basic Specification 1.0
  - Supports Target Reset Action (RSTACT) CCC from MIPI I3C Specification 1.1
  - Supports Dynamic Address Assignment, Common Command Codes (CCC), Direct and Broadcast addressing
  - Transfer speeds up to 12.5 Mbps in SDR mode
  - Recognizes HDR Entry and Exit patterns
  - Support for In-Band Interrupt (IBI) and Hot-Join

- Supports 7-bit configurable target static address
- I<sup>2</sup>C backward-compatible with static addressing for I<sup>2</sup>C transfers
- Built-in Error Detection and Recovery
- Device I/O Port Features:
  - 11 I/O pins including two Multi-Voltage I/O (MVIO) pins powered by V<sub>DDIO2</sub> (PIC18F04/05/06Q20)
  - 16 I/O pins including two Multi-Voltage I/O (MVIO) pins powered by V<sub>DDIO2</sub> and two MVIO pins powered by V<sub>DDIO3</sub> (PIC18F14/15/16Q20)
  - MVIO pins support a voltage range of 1.62V through 5.5V
  - Support for 0.95-3.63V I3C communication at up to 12.5 MHz on MVIO pins
  - Individually programmable I/O direction, open-drain, slew rate and weak pull-up control
  - Low-Voltage interface on all I/O pins using LVBUF input buffer
  - Selectable I3C and I<sup>2</sup>C input buffers on MVIO pins
  - Interrupt-on-change on most pins
  - Three programmable external interrupt pins
- One Signal Routing Port Module:
  - 8 signal routing pins per module
  - Supports software read/write and customizable input/output control
  - Supports flip-flops and clock source selection for Hardware State Machine and shift register applications
  - Integration with PPS, Interrupt-on-Change and DMA/ADC triggers available
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O (except I3C signals)

## Analog Peripherals

- 10-Bit Analog-to-Digital Converter with Computation (ADCC):
  - Up to 11 external channels and five internal channels
  - Supports grouping of external channels
  - Up to 300 ksps
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Five internal analog channels
  - Hardware Capacitive Voltage Divider (CVD) Support:
    - Adjustable Sample-and-Hold capacitor array
    - Guard ring digital output drive
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
  - Internal connections to ADC

## Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz

- $\pm 1\%$  at calibration
  - Active Clock Tuning of HFINTOSC for better accuracy
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-Frequency Oscillator Block:
  - Configurable HS Crystal mode up to 32 MHz
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if external clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources

### **Programming/Debug Features**

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

# PIC18-Q20 Block Diagram

